

CONFUCIUS

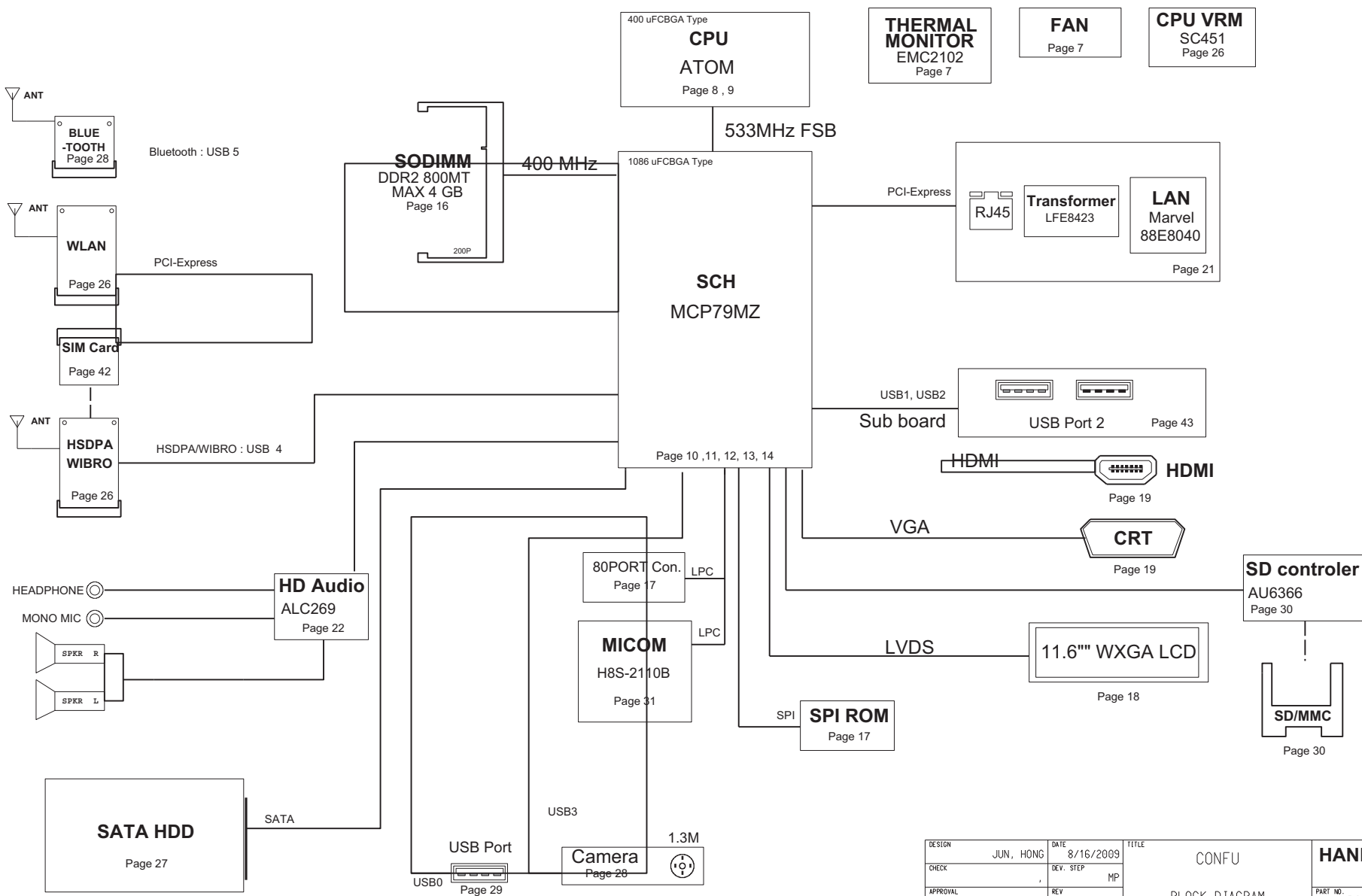
CPU :ATOM (N270)
Chip Set :MCP79MZ
Remarks :12.1"

Model Name : CONFU
PBA Name : PBA01-0010A
PCB Code : PCB01-0010A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2009.09.05

DESIGN	CHECK	APPROVAL

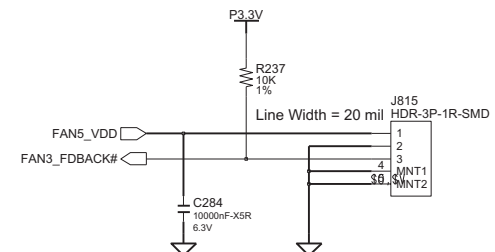
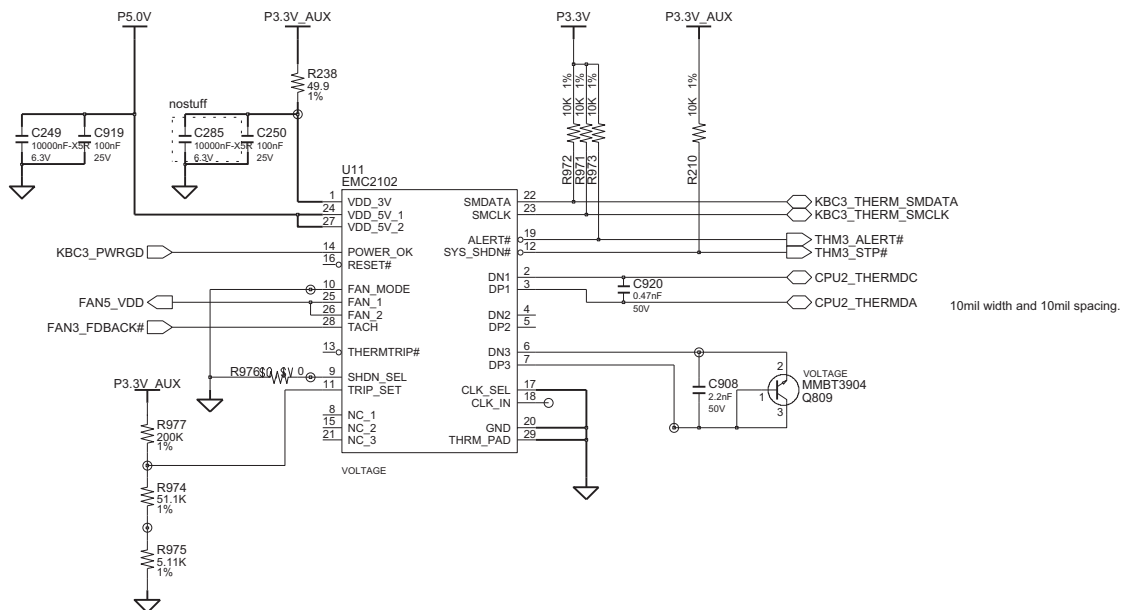
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APPROVAL		REV	1.0	TOC		PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 12:40:05 AM	PAGE	1	OF 40

OPERATION BLOCK DIAGRAM



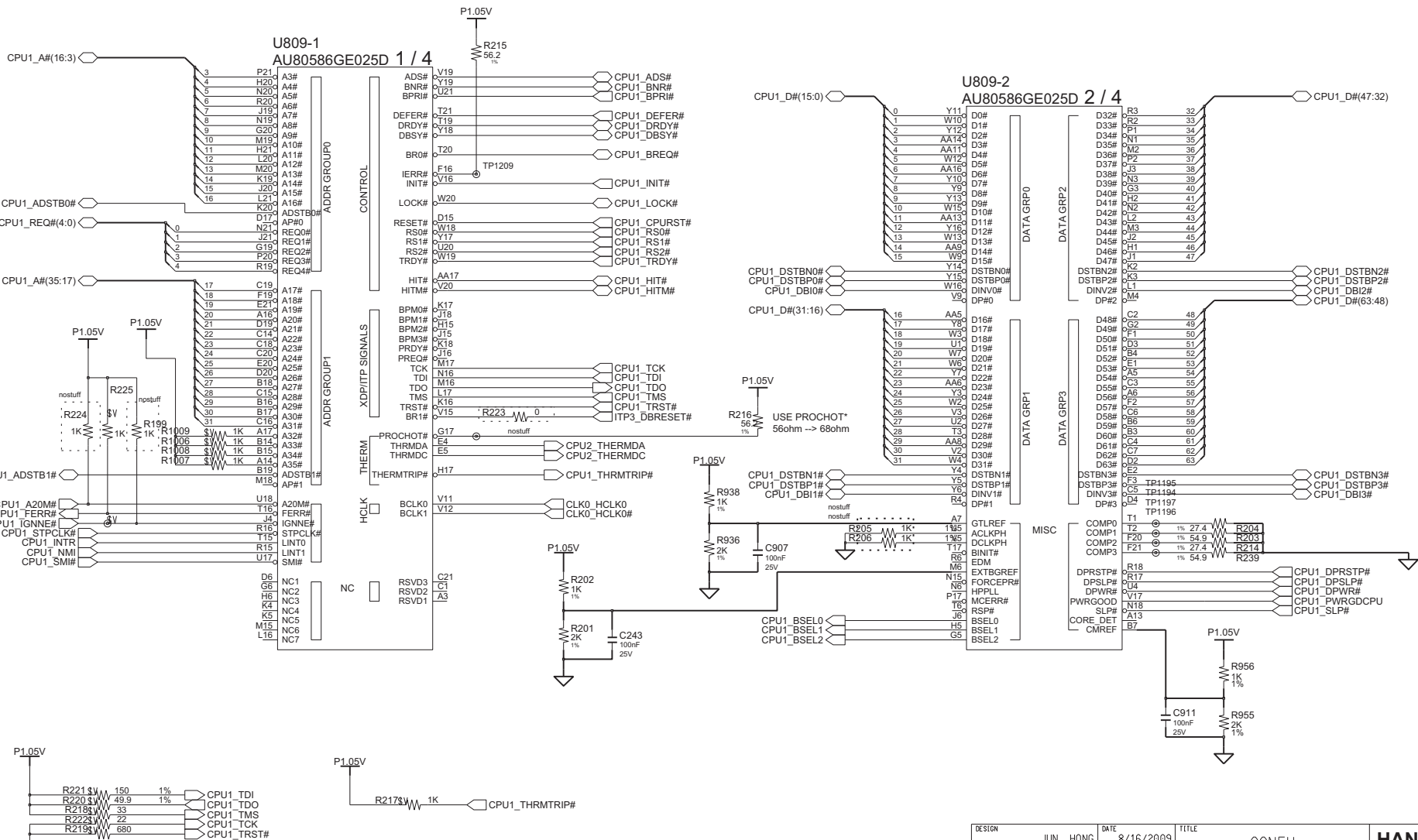
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MODULE CODE		LAST EDIT	August, 16, 2009 1:20:51 PM		
				PAGE	2 OF 40

THERMAL IC



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK TECH PART NO. PCB01-0010A
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APPROVAL		REV	1.0		THERMAL SENSOR & FAN CONTROL	
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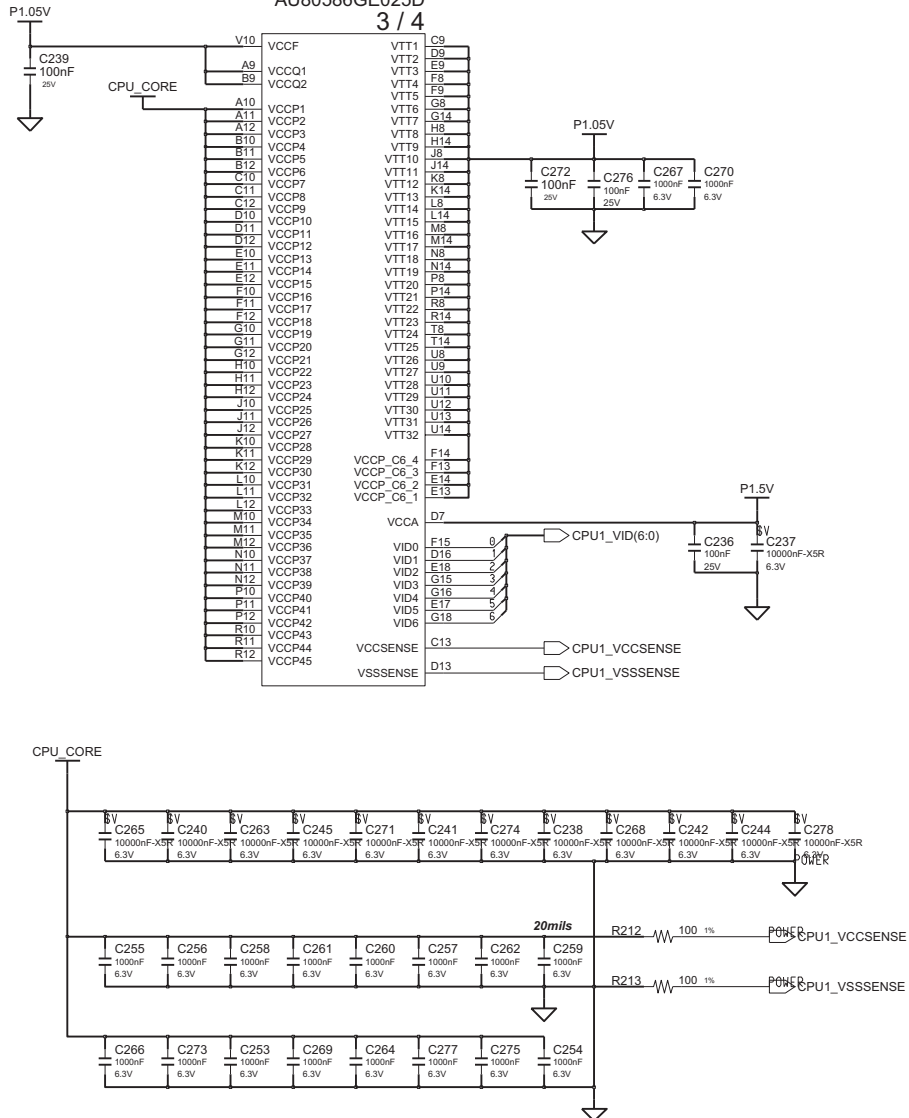
CPU : (N270)



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		CONFU		HANDBOOK	
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APPROVAL		REV	1.0	CPU 1/2		PART NO.		TECH	
MODULE CODE	LAST EDIT					August, 16, 2009 1:25:00 PM		PAGE	8
						PCB01-0010A			

DIAMONDVILLE (N270)

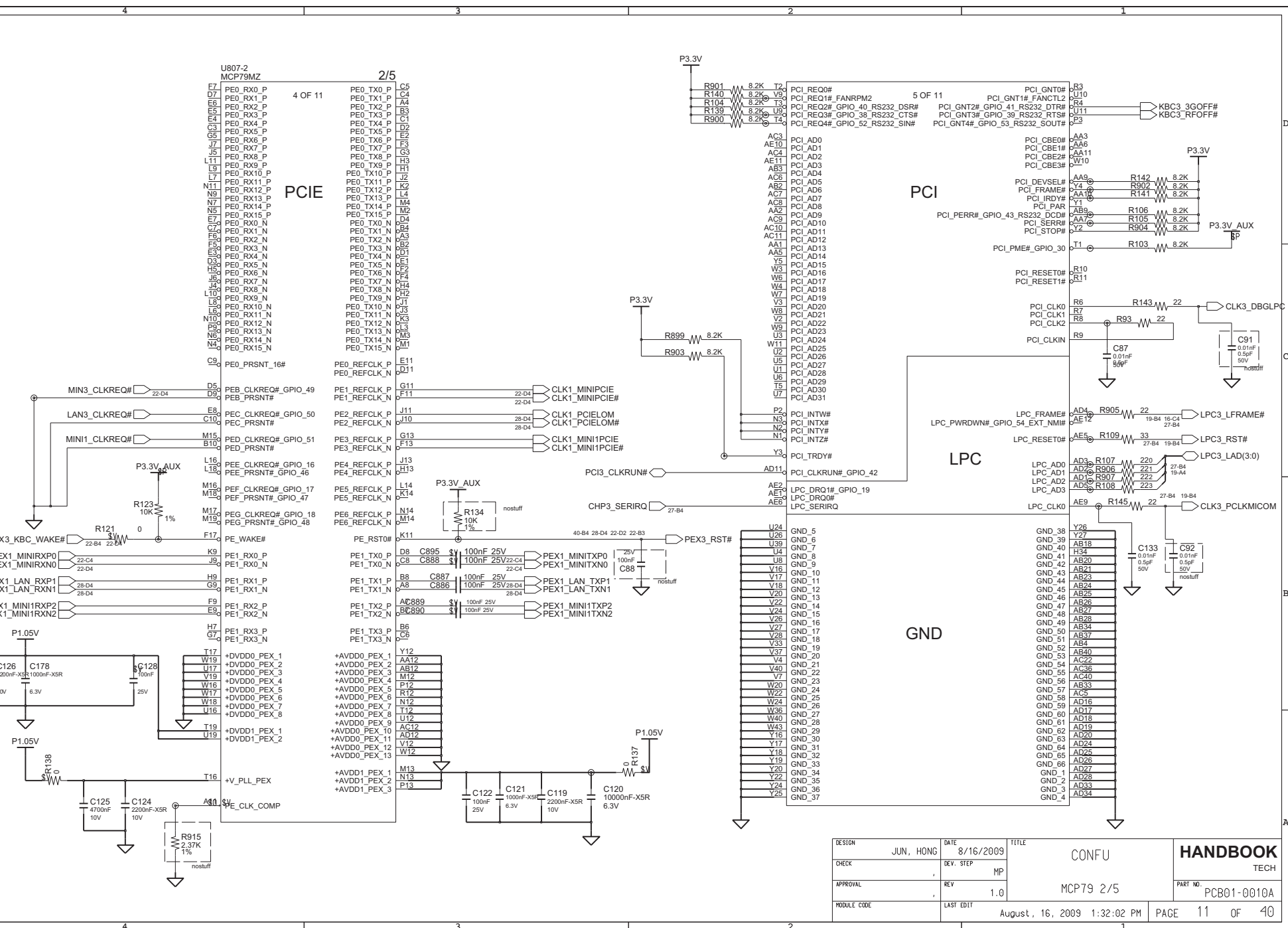
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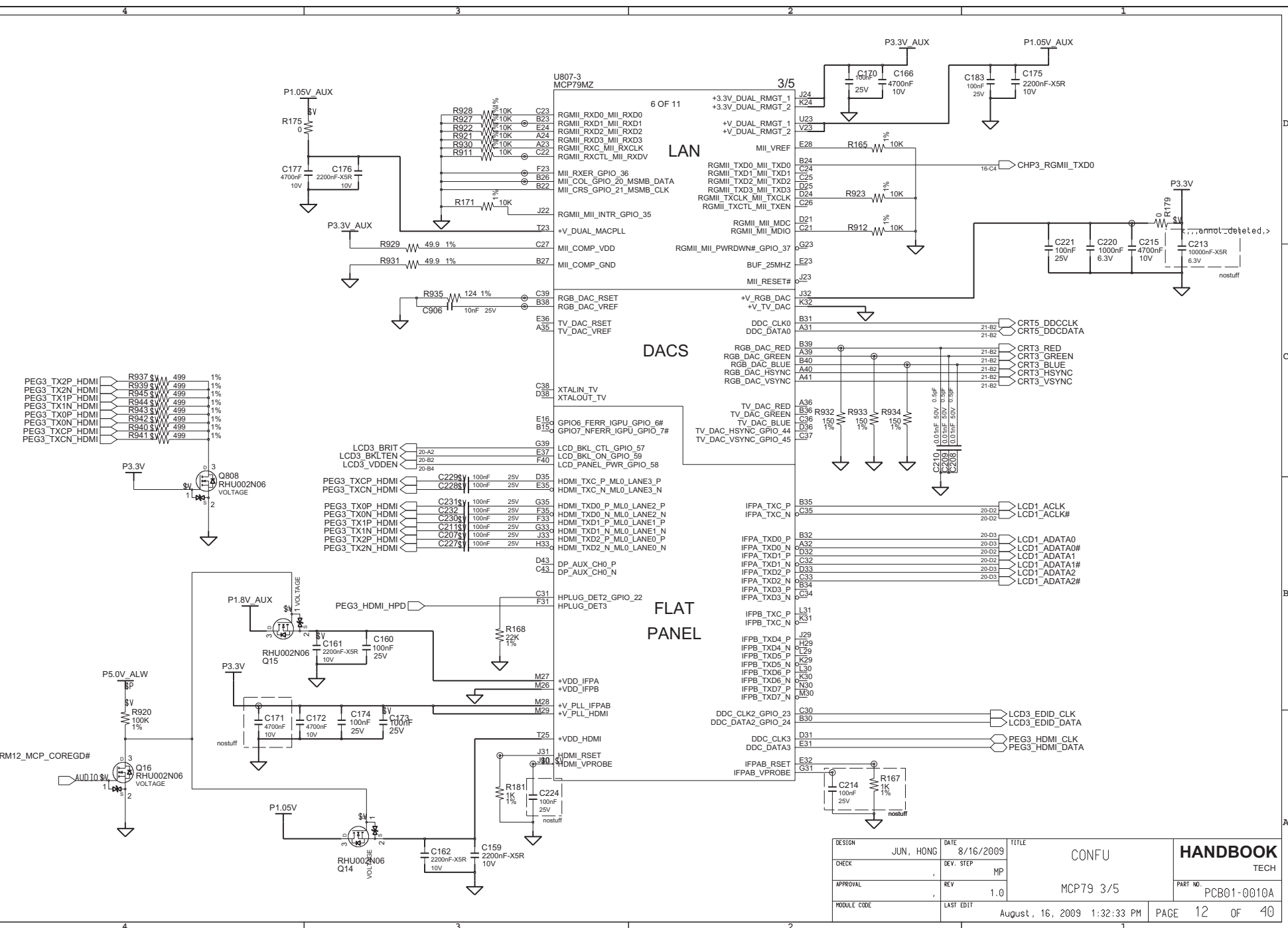


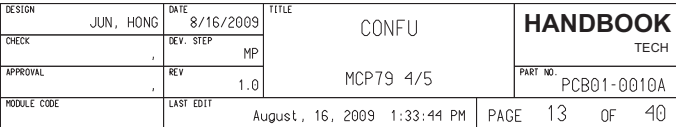
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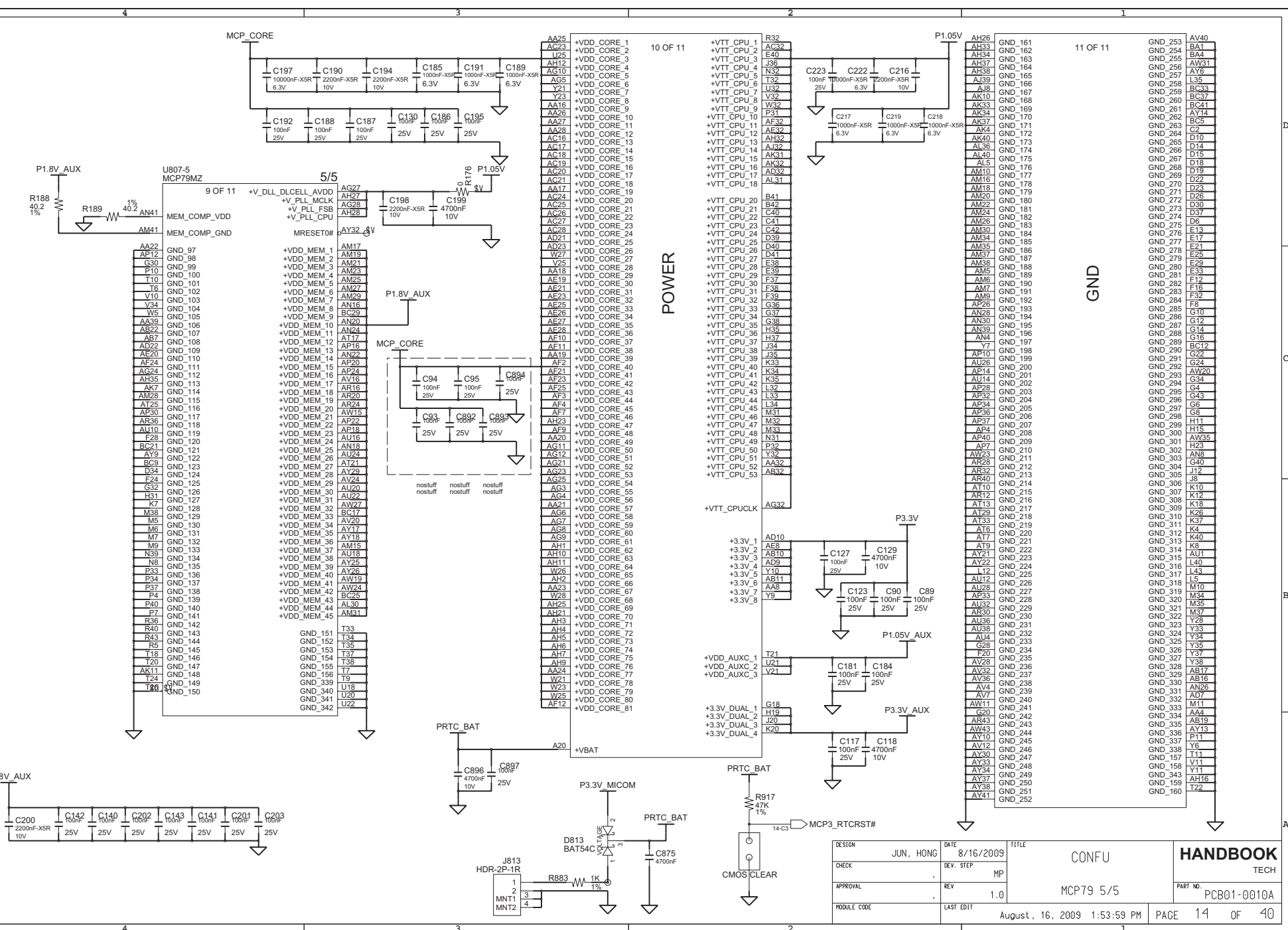
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A20	VSS7	AA7
B1	VSS8	AA4
B2	VSS9	AA3
B5	VSS10	AA2
B6	VSS11	Y21
B13	VSS12	Y20
B20	VSS13	Y2
B21	VSS14	Y1
C9	VSS15	W21
C17	VSS16	W17
D1	VSS17	W14
D5	VSS18	W11
D8	VSS19	W8
D14	VSS20	W5
D18	VSS21	W1
D21	VSS22	V21
E3	VSS23	V18
E6	VSS24	V14
E7	VSS25	V13
E8	VSS26	V8
E15	VSS27	V7
E16	VSS28	V6
E19	VSS29	V4
F4	VSS30	V1
F5	VSS31	U19
F6	VSS32	U16
F7	VSS33	U15
F17	VSS34	U7
F18	VSS35	U6
G1	VSS36	U3
G4	VSS37	T18
G7	VSS38	T13
G9	VSS39	T12
G13	VSS40	T11
G21	VSS41	T10
H3	VSS42	T9
H4	VSS43	T7
H7	VSS44	T5
H9	VSS45	T4
H13	VSS46	R21
H16	VSS47	R13
H18	VSS48	R9
H19	VSS49	R7
J5	VSS50	R5
J7	VSS51	R1
J9	VSS52	P19
J13	VSS53	P18
J17	VSS54	P16
K1	VSS55	P15
K6	VSS56	P13
K7	VSS57	P9
K9	VSS58	P7
K13	VSS59	P6
K15	VSS60	P5
K21	VSS61	P3
L3	VSS62	N17
L4	VSS63	N13
L5	VSS64	N13
L6	VSS65	N9
L7	VSS66	N7
L9	VSS67	N4
L13	VSS68	M21
L15	VSS69	M13
L18	VSS70	M3
L19	VSS71	M7
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DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK TECH PART NO. PCB01-0010A
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APPROVAL		REV	1.0		CPU 2/2	
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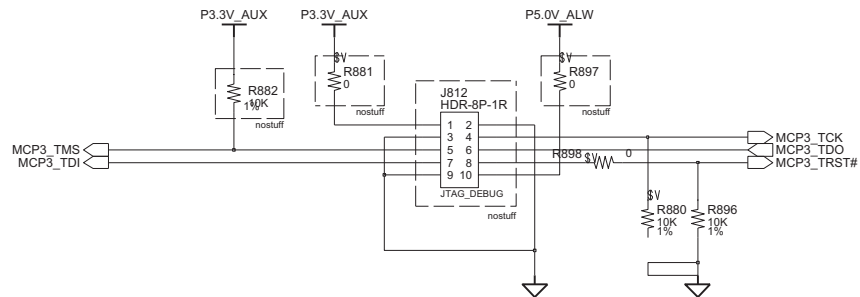
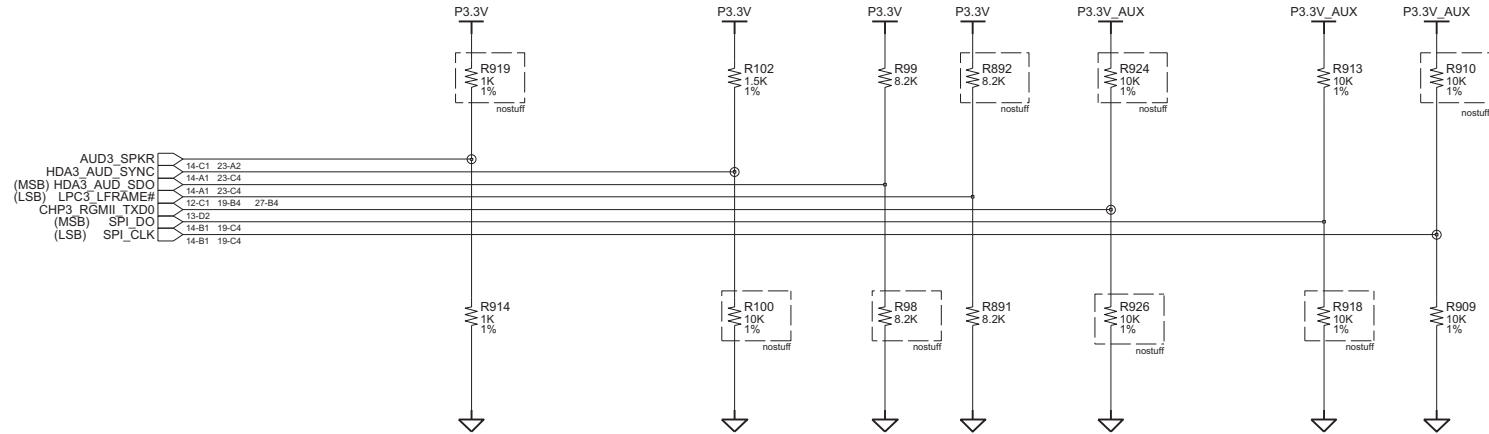






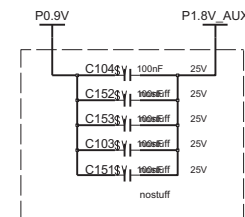
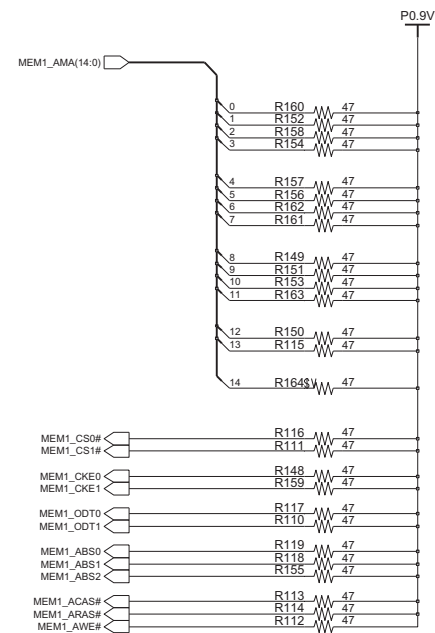
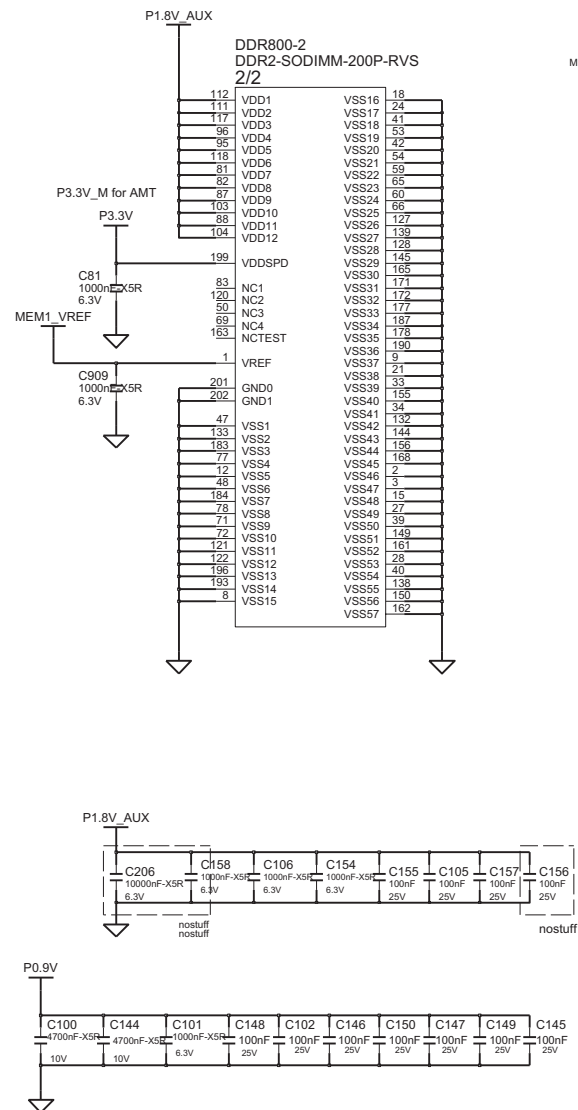
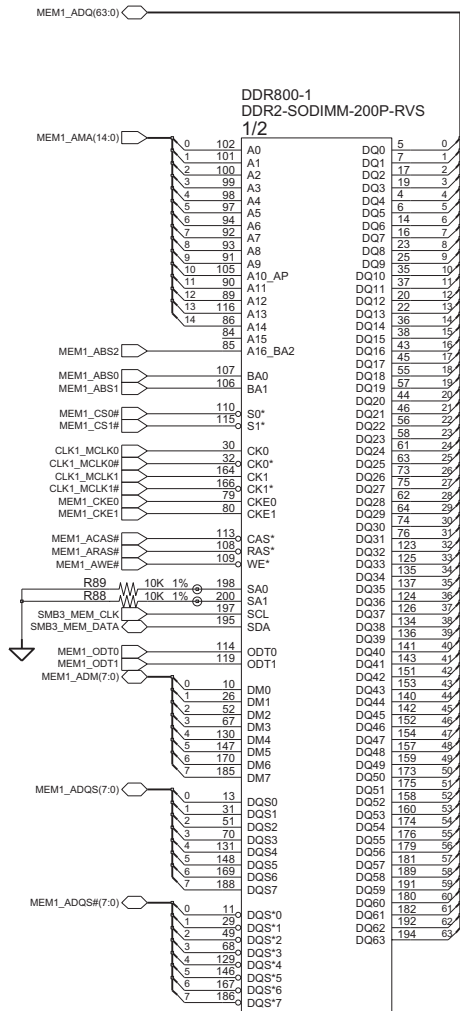
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MODULE CODE		LAST EDIT		August, 16, 2009 1:53:59 PM		PAGE	14 OF 40	

REQUIRED SYSTEM STRAPS



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK TECH PART NO. PCB01-0010A
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APPROVAL		REV	1.0		REQUIRED SYSTEM STRAPS	
MODULE CODE		LAST EDIT	August, 16, 2009 1:56:49 PM	PAGE	15 OF 40	

DDR SO-DIMM #0



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		HANDBOOK TECH		
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APPROVAL		REV	1.0	DDR SO-DIMM			PART NO.	PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 2:08:37 PM		PAGE		16	OF 40

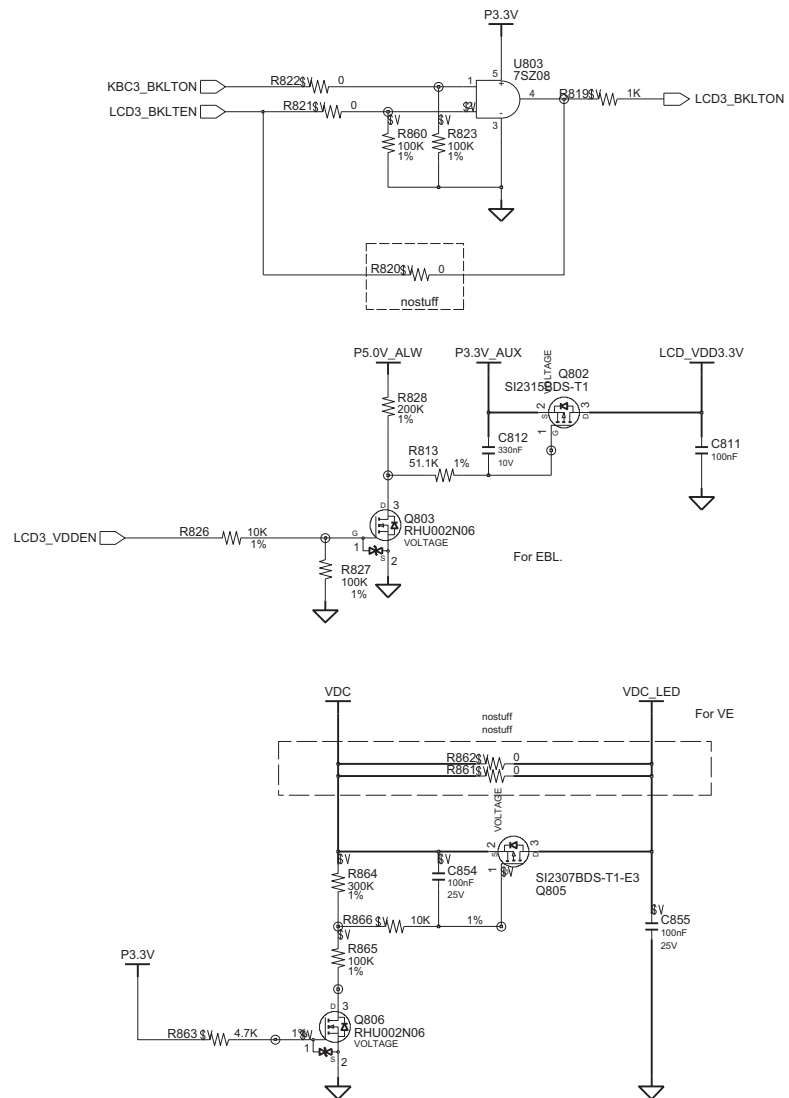
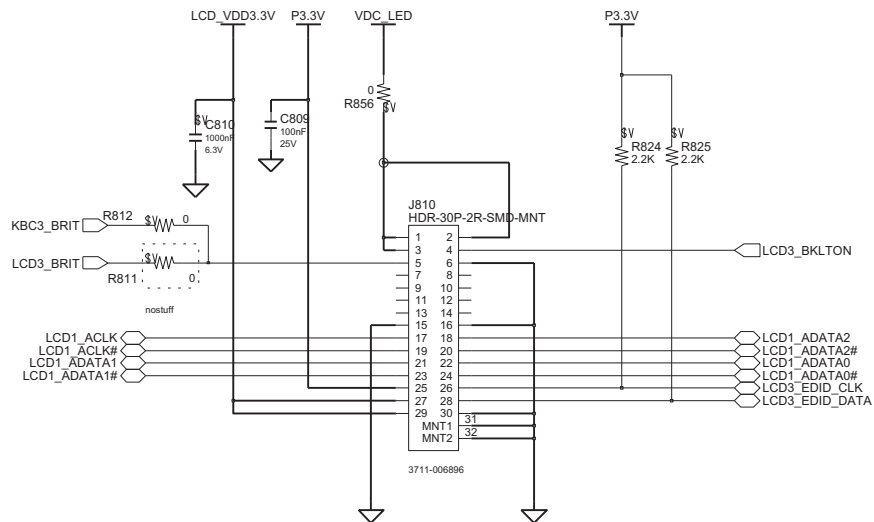
[illegible]

Pin connection diagram for the LPC3114 microcontroller. The diagram shows the microcontroller's pins connected to a P3.3V supply and a J819 HDR-10P-SMD connector. The connections are:

- LPC3_RST# to pin 1
- CLK3_DBG LPC to pin 2
- LPC3_LFRAME# to pin 3
- LPC3_LAD(3) to pin 4
- LPC3_LAD(2) to pin 5
- LPC3_LAD(1) to pin 6
- LPC3_LAD(0) to pin 7
- P3.3V to pin 8
- MNT1 to pin 9
- MNT2 to pin 10

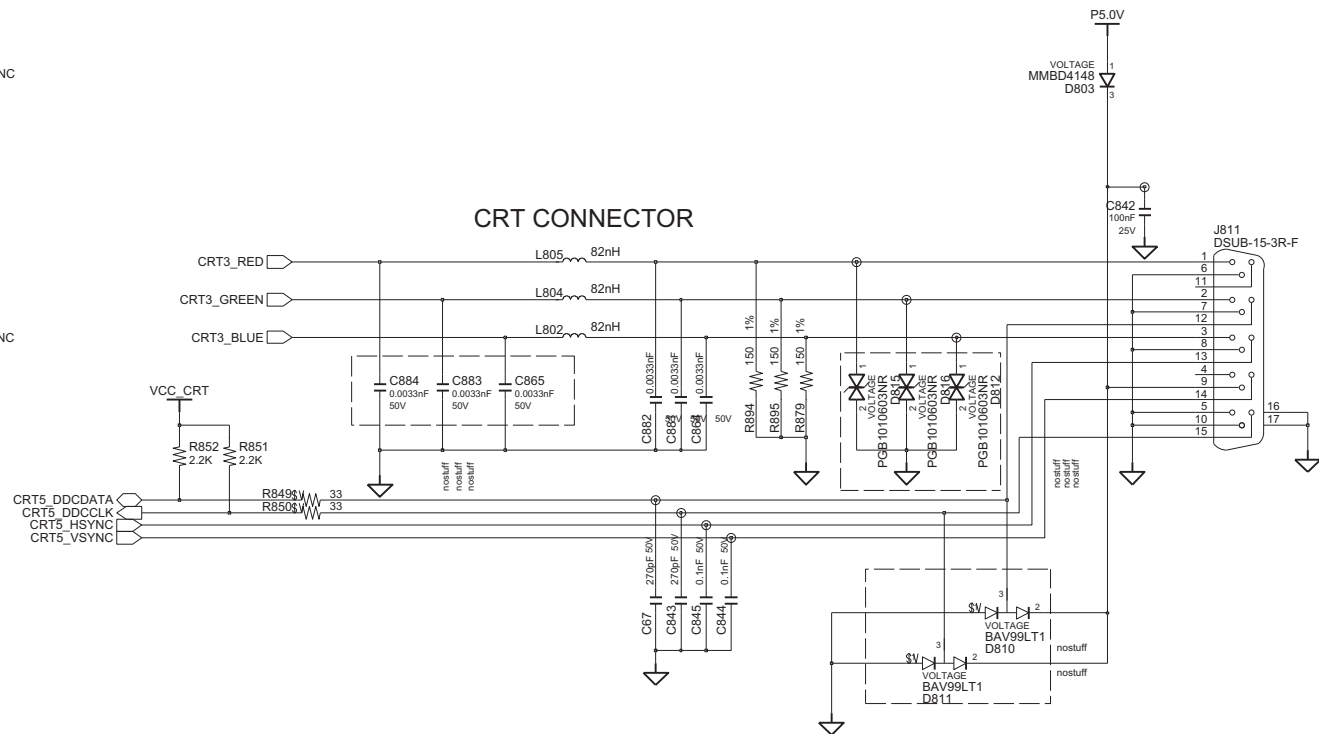
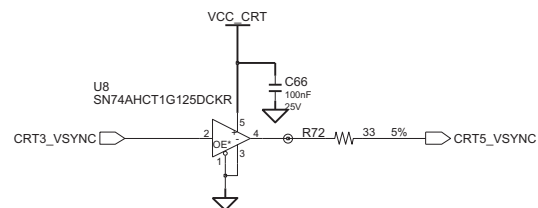
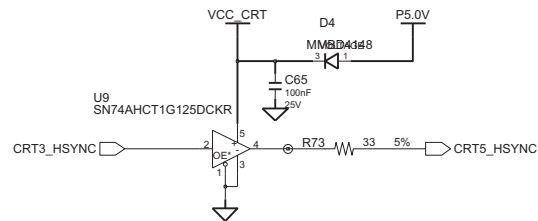
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
36	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY * PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DESIGN	JUN, HONG	DATE	8/16/2009	TITLE CONFU BOIS		HANDBOOK		
CHECK	'	DEV. STEP	MP			TECH		
APPROVAL	'	REV	1.0			PART NO.	PCB01-0010A	
MODULE CODE		LAST EDIT		August, 16, 2009 2:09:27 PM	PAGE	17	OF	40



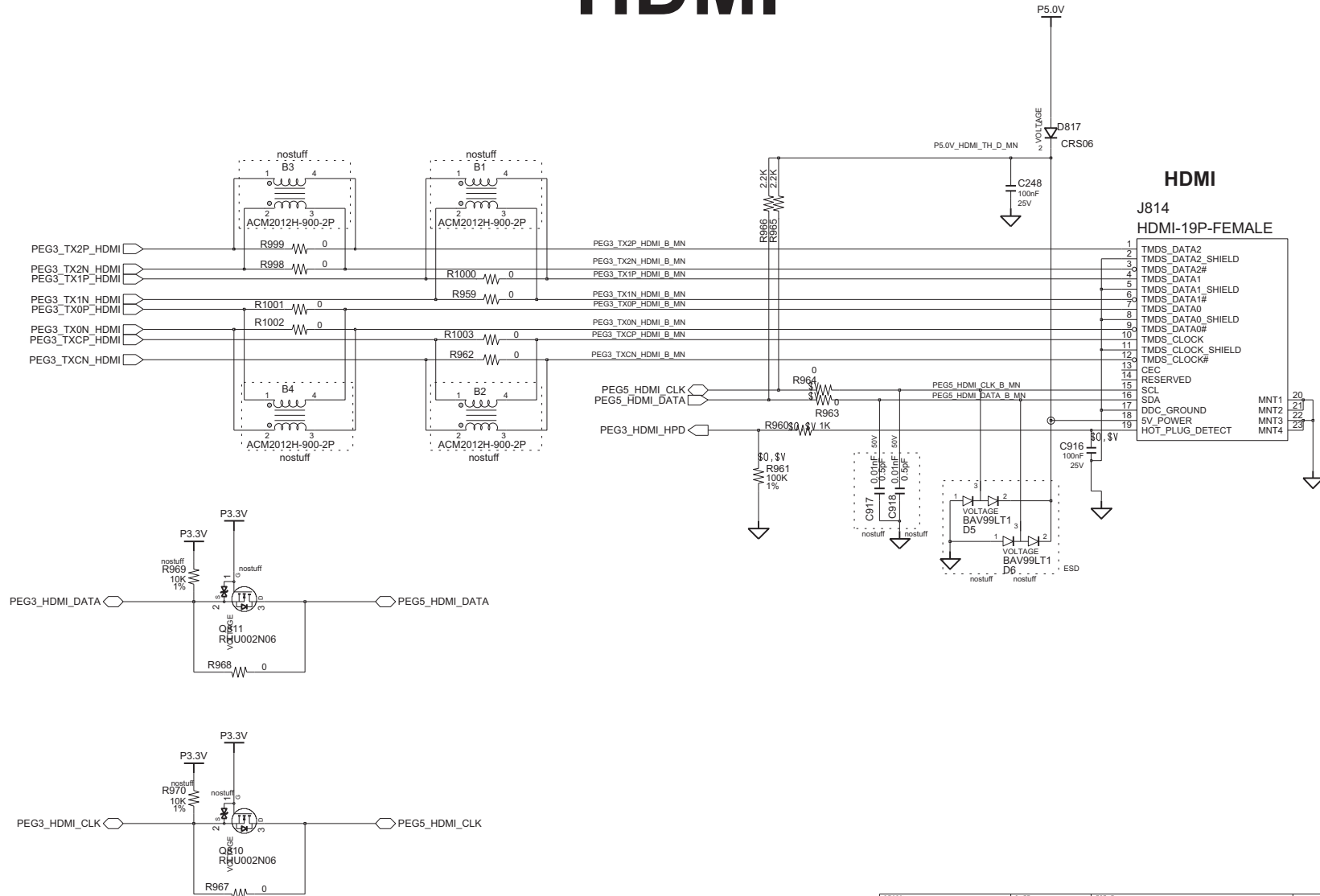
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CRT I/F



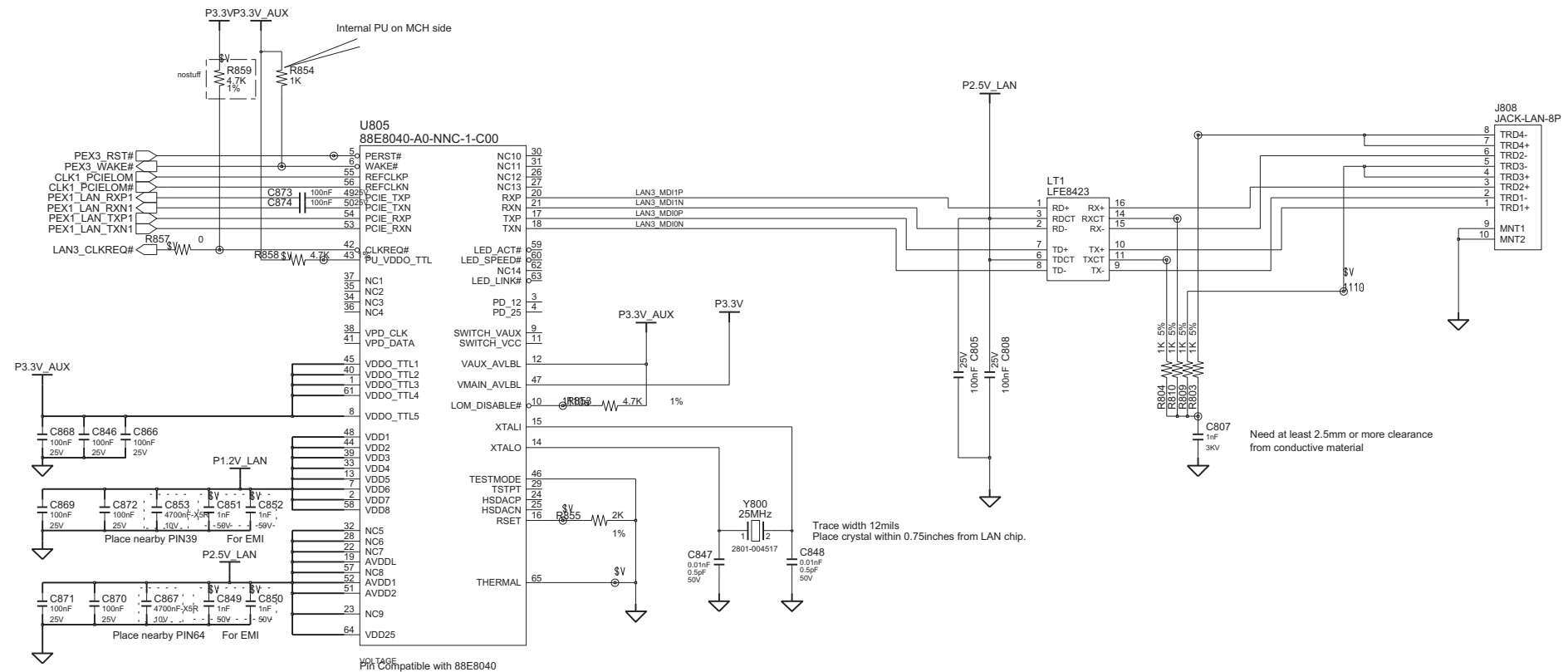
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HDMI



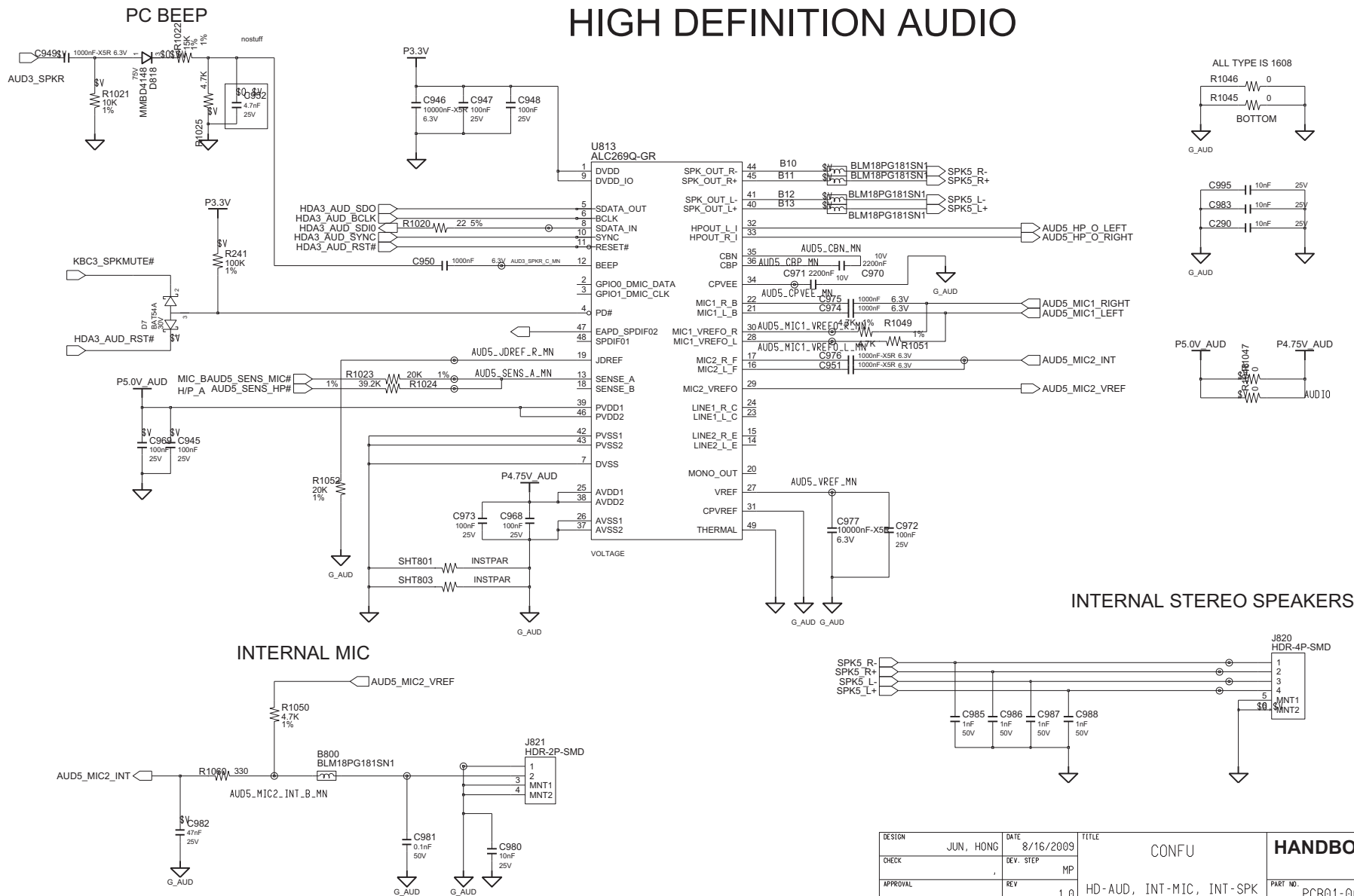
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Marvell 88E8040 (WIRED LAN)



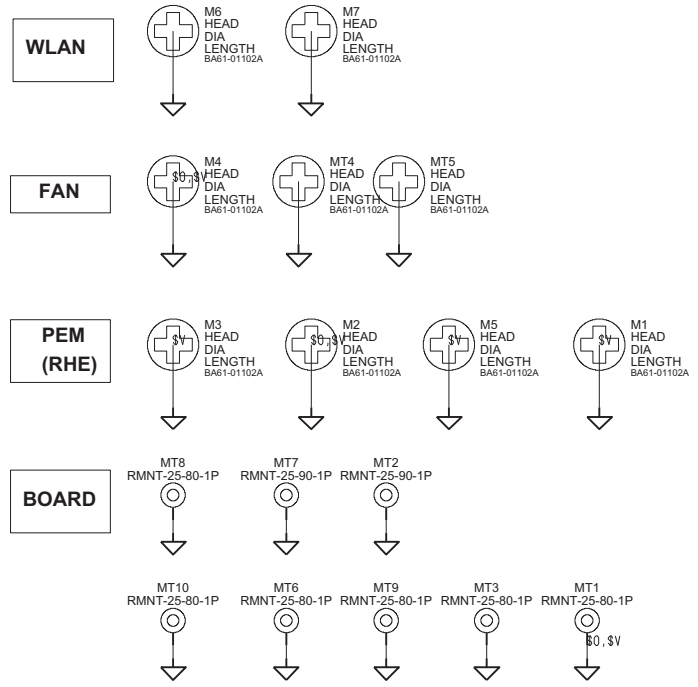
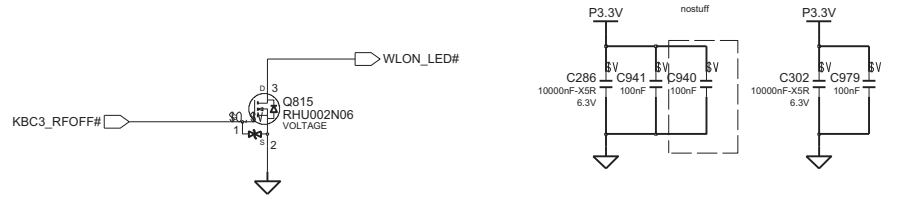
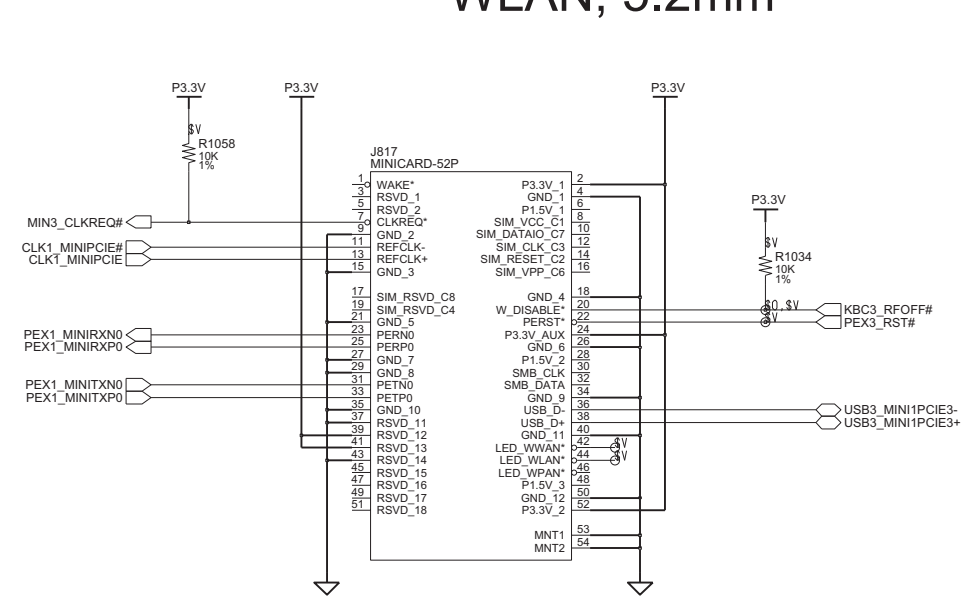
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HIGH DEFINITION AUDIO

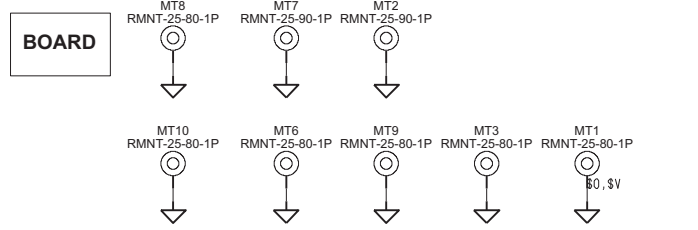
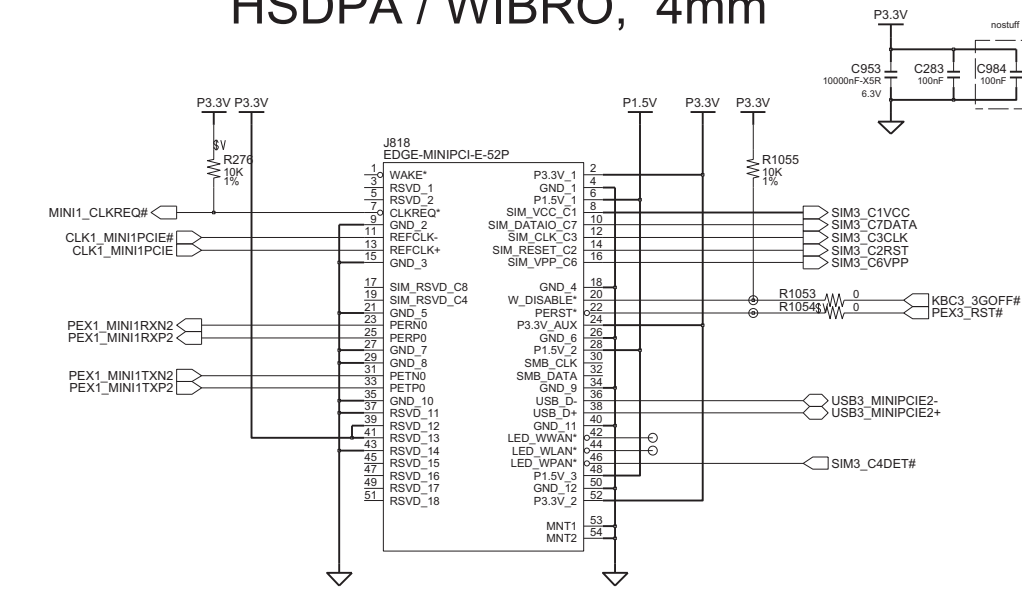


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WLAN, 5.2mm

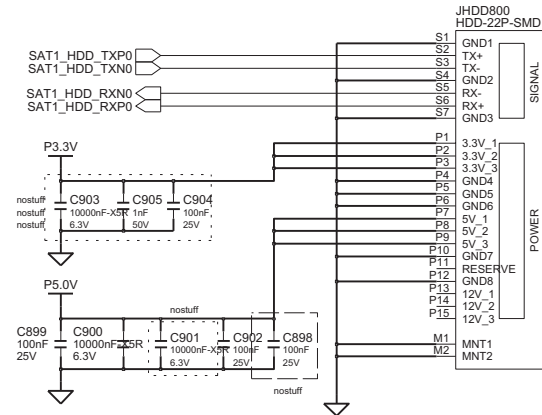


HSDPA / WIBRO, 4mm



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				PAGE	23	OF 40

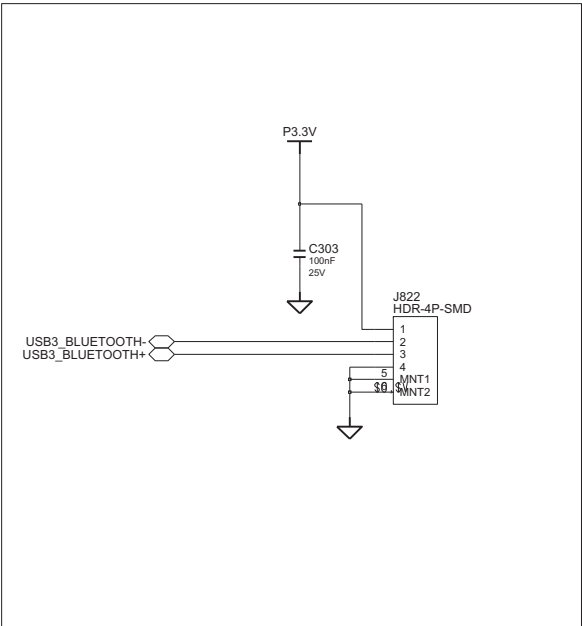
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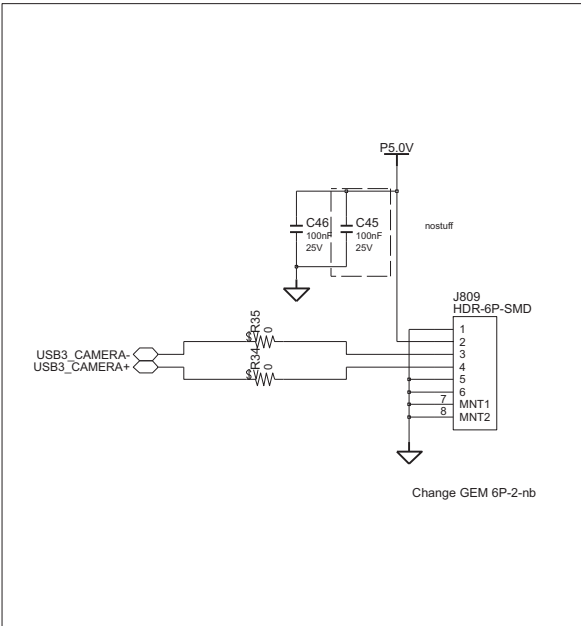
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USB I/F Devices

Bluetooth Interface



CAMERA



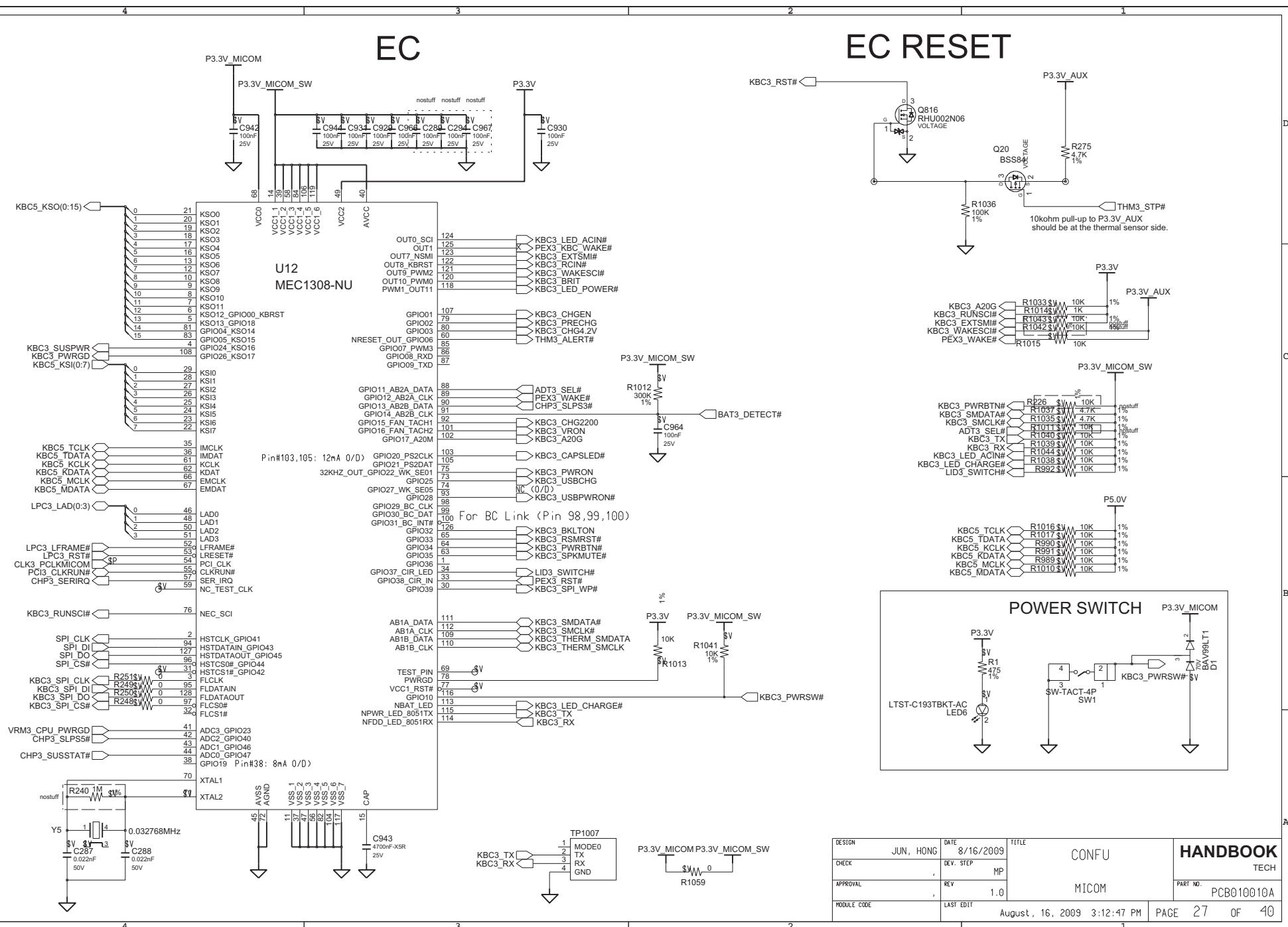
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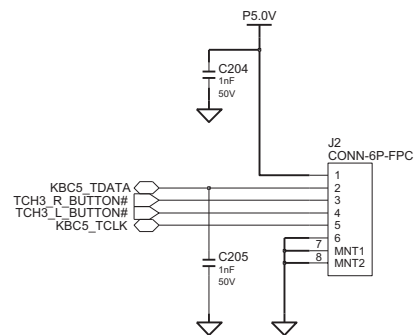
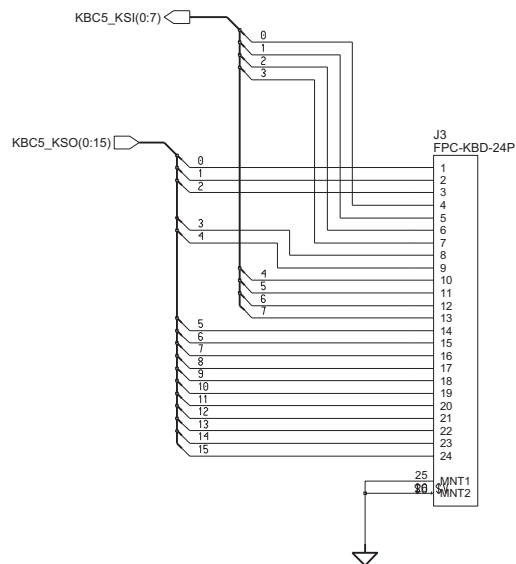


P3.3V MICOM

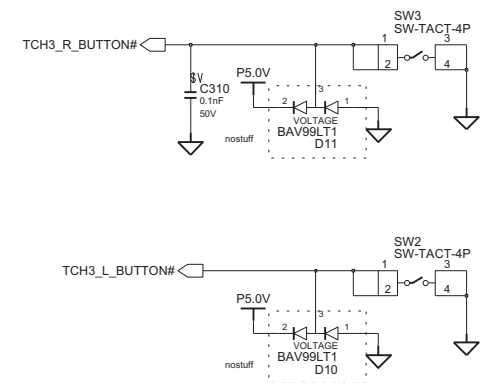




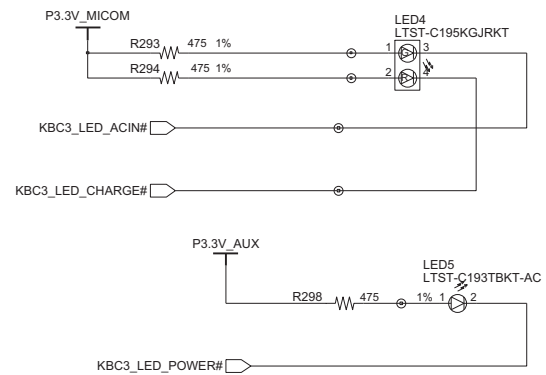
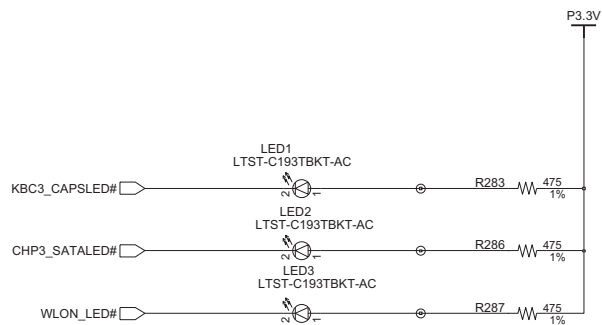
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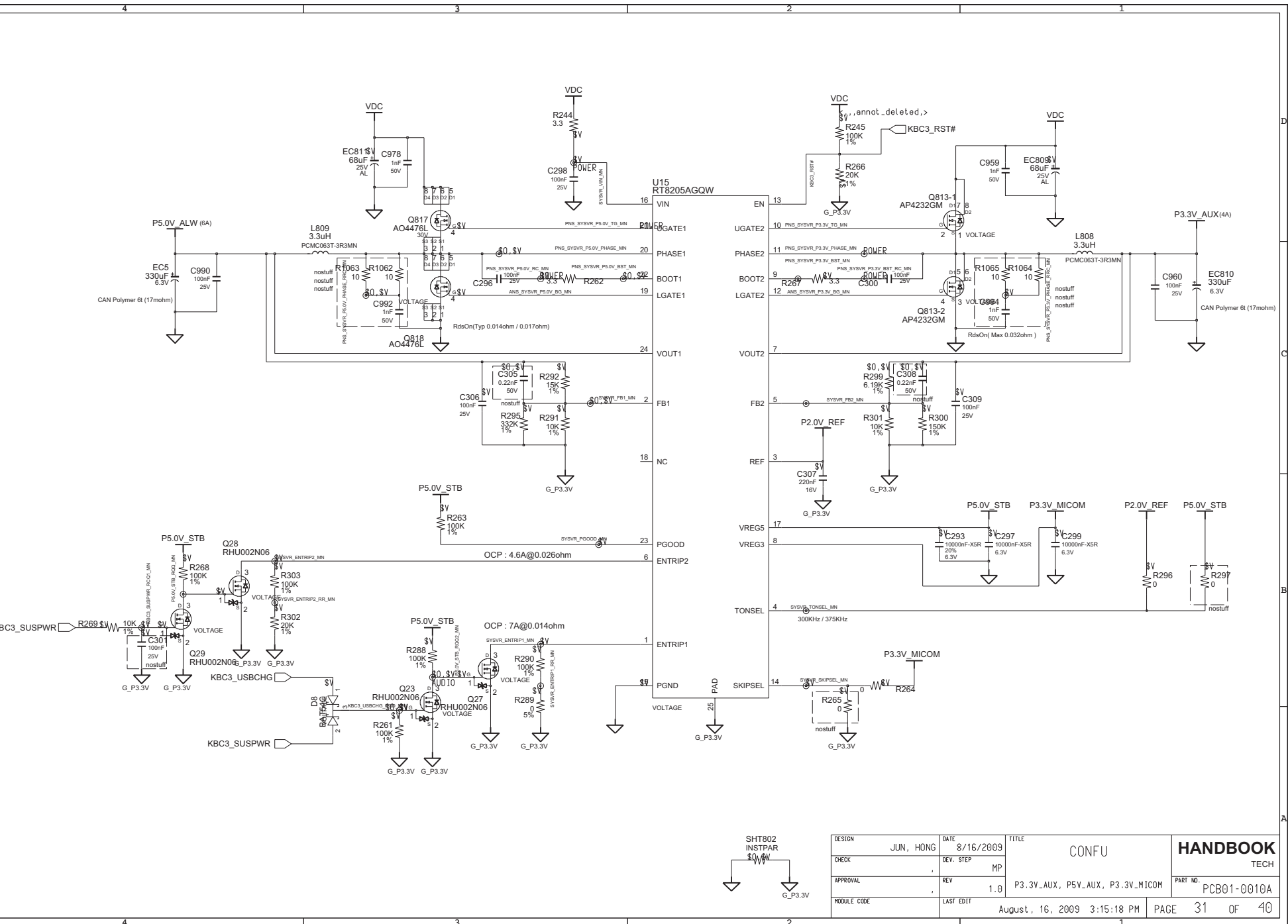
TOUCHPAD



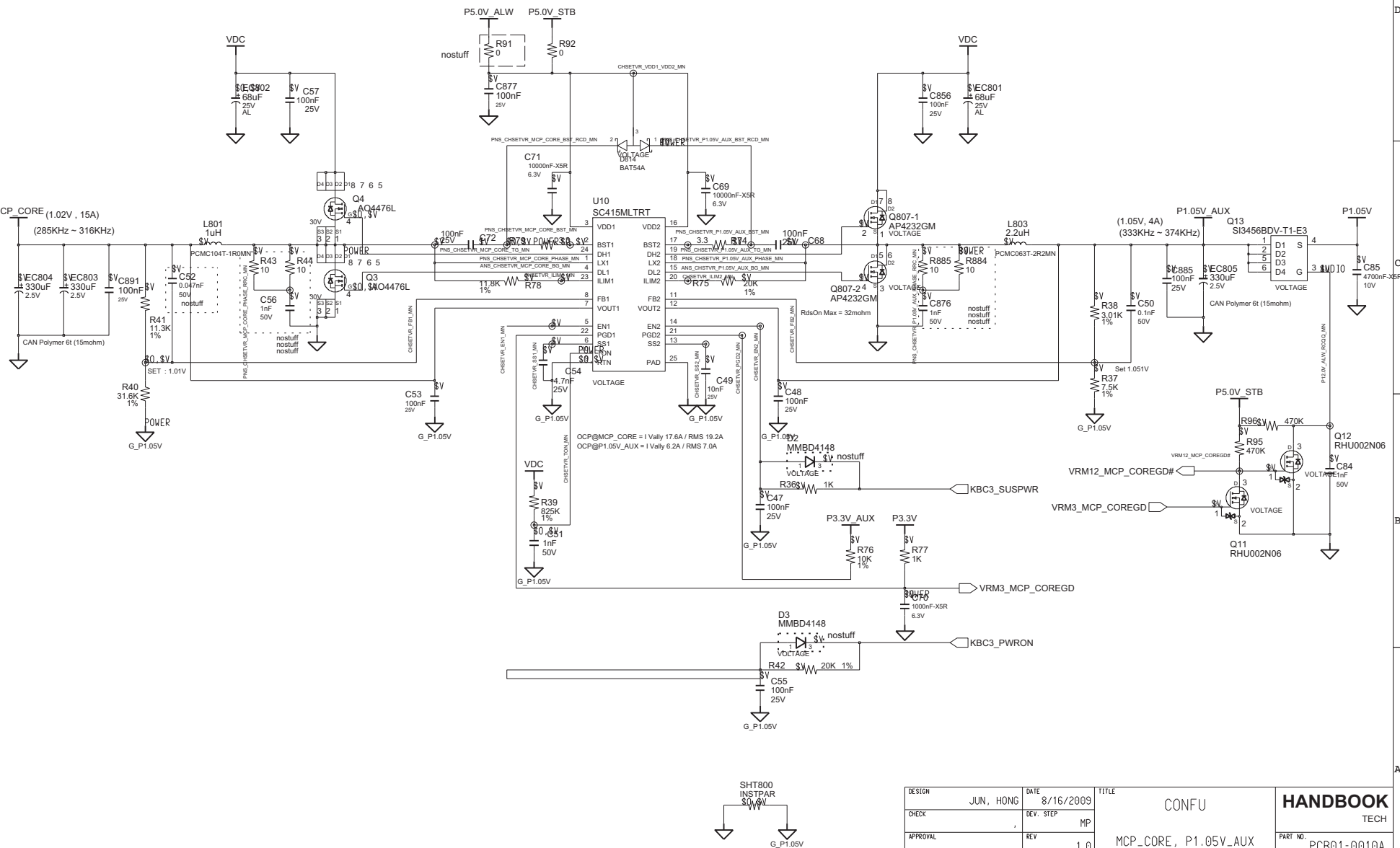
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MODULE CODE		LAST EDIT	August, 16, 2009 3:13:12 PM	PAGE	28	OF 40



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MCP_CORE & P1.05V_AUX

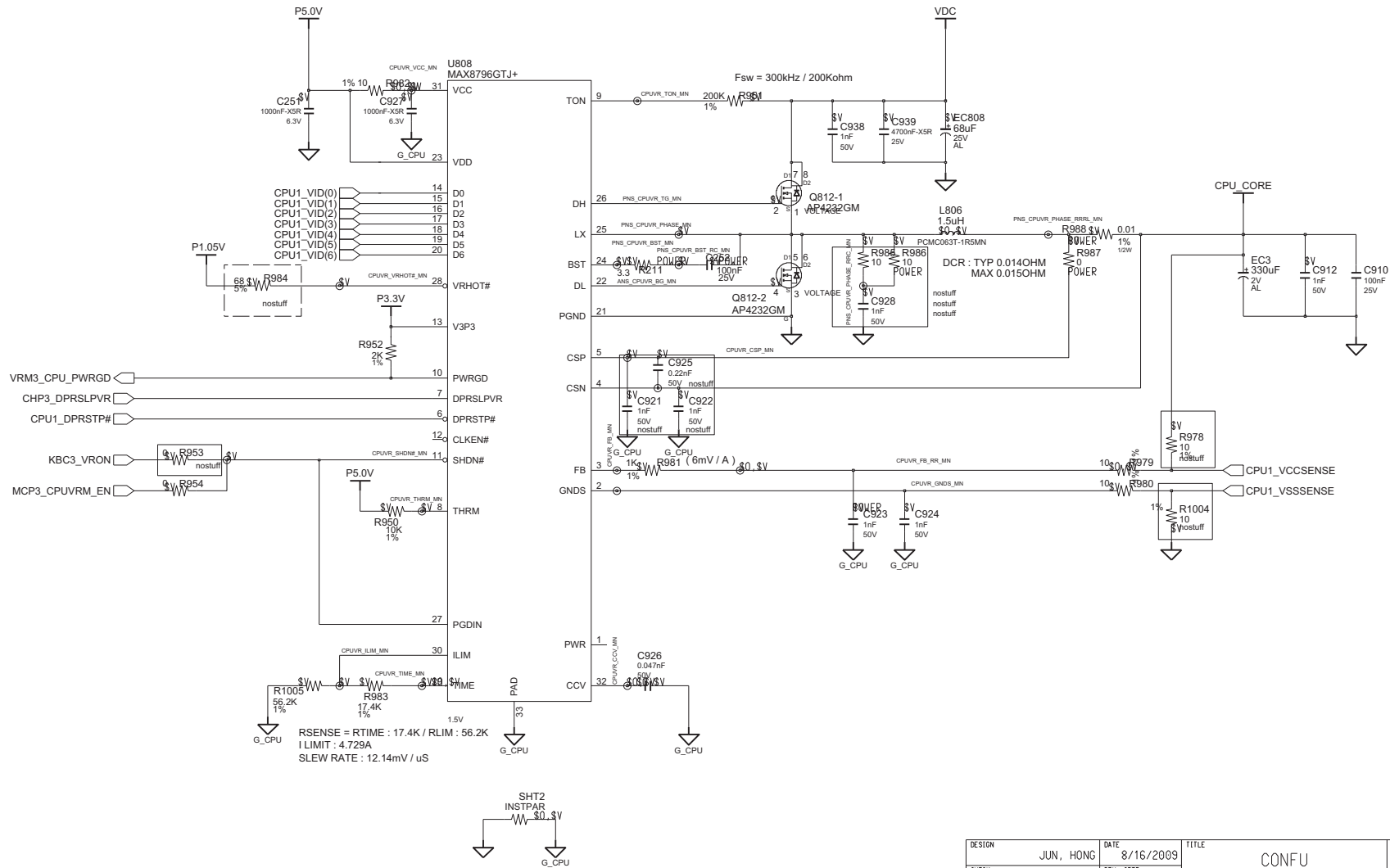


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MODULE CODE		LAST EDIT		August, 16, 2009 3:15:49 PM		PAGE	32 OF 40

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CPU VRM POWER

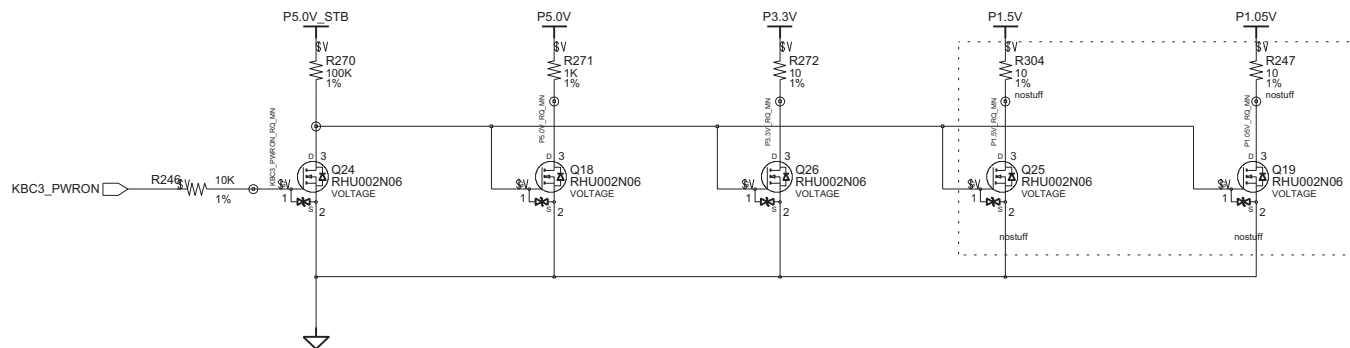


The schematic diagram illustrates the power supply section of the KBC3-PWR0N module. The input is a 40-A4 signal, which passes through a 10K resistor (R1031) and a network of capacitors (C961: 25V, 100nF, noisstuff) and resistors (R1029: 100K, 1%, R1030: 10K, 1%) connected to ground. The main power path goes through a diode Q814 (RHU02N06) and a MOSFET AO6409 (U812) to a 3.3V_AUX output. A 10V capacitor C963 (2200nF-X5R) is connected to the 3.3V_AUX output. A 3.3V output is also shown with a 10V capacitor C963.

The schematic diagram illustrates the power supply and signal connections for the SHT800 module. The module is represented by a 40-44 pin connector. The power supply section includes a 5V regulator (Q22) connected to P5.0V_ALW and P5.0V_AUD. The signal section shows three signal pins (INSTPAR, INSTPAR, INSTPAR) connected to SHT806, SHT805, and SHT804 respectively. The diagram also shows various passive components like resistors (R1061, R284, R285) and capacitors (C991, C993, C295).

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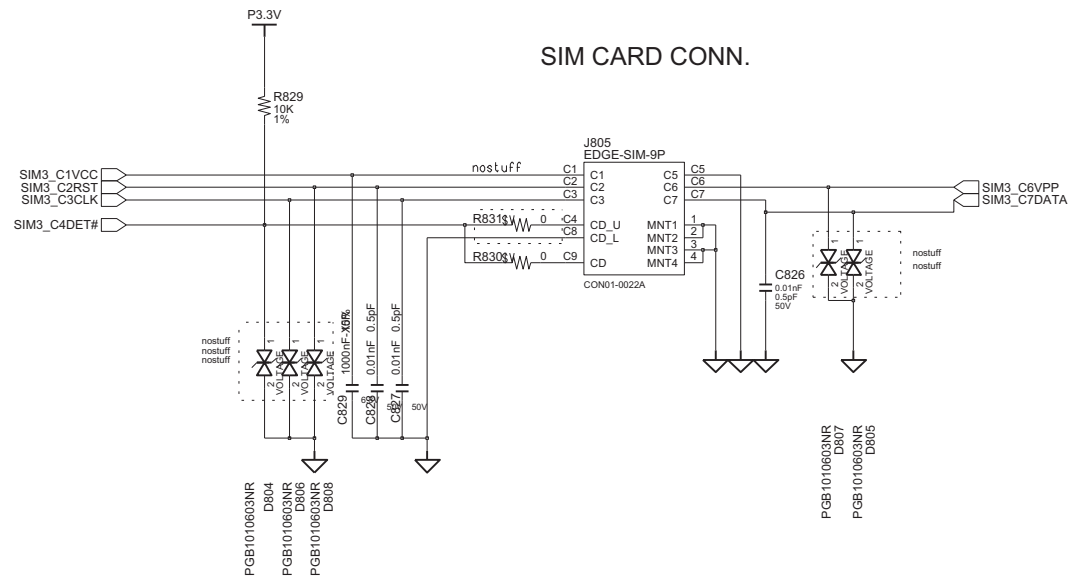
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CHECK	,	REV. STEP	MP				
APPROVAL	,	REV	1.0	LOAD SW CONTROL		PART NO.	PCB01-0010A
MODULE CODE	LAST EDIT		August, 16, 2009 3:16:43 PM			PAGE	35 OF 40



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		CONFU		HANDBOOK	
CHECK	,	DEV. STEP	MP						
APPROVAL	,	REV	1.0	DISCHARGER		PART NO.		TECH	
						PCB01-0010A			
MODULE CODE		LAST EDIT		August, 16, 2009 3:17:00 PM		PAGE	36	OF	40

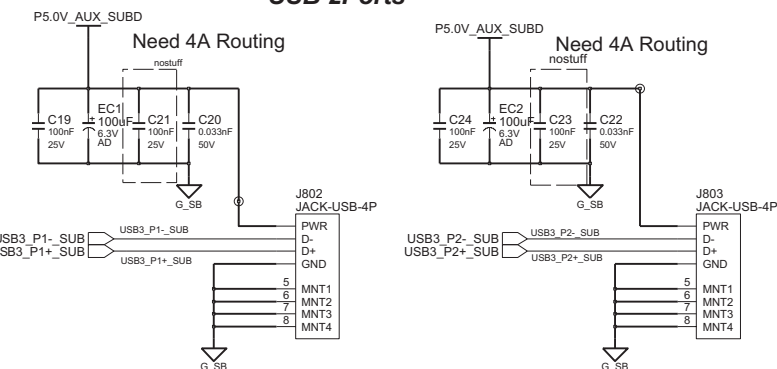
SIM Card

SIM CARD CONN.

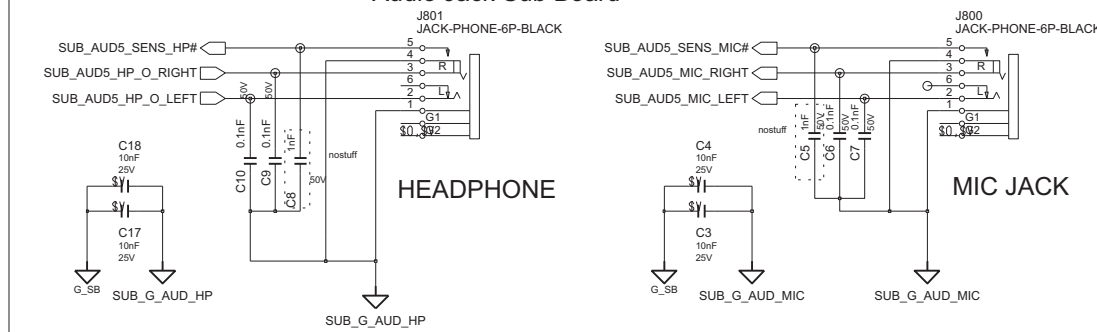


DESIGN	JUN, HONG	DATE	8/16/2009	CONFU		HANDBOOK
CHECK		DEV. STEP	MP			
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MODULE CODE		LAST EDIT	August, 16, 2009 3:17:23 PM			PAGE
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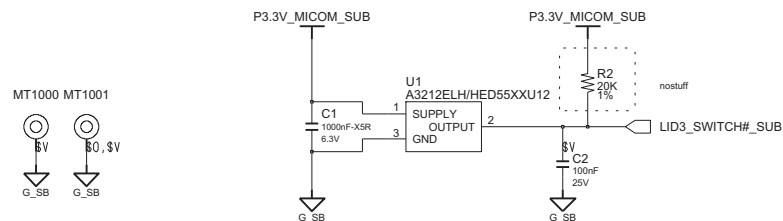
SUB Board (USB 2Ports, Audio 2Ports, MMC)

USB 2Ports

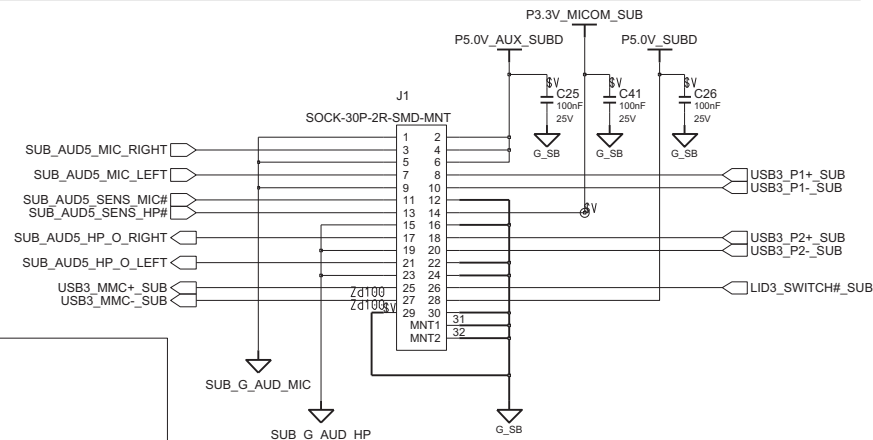
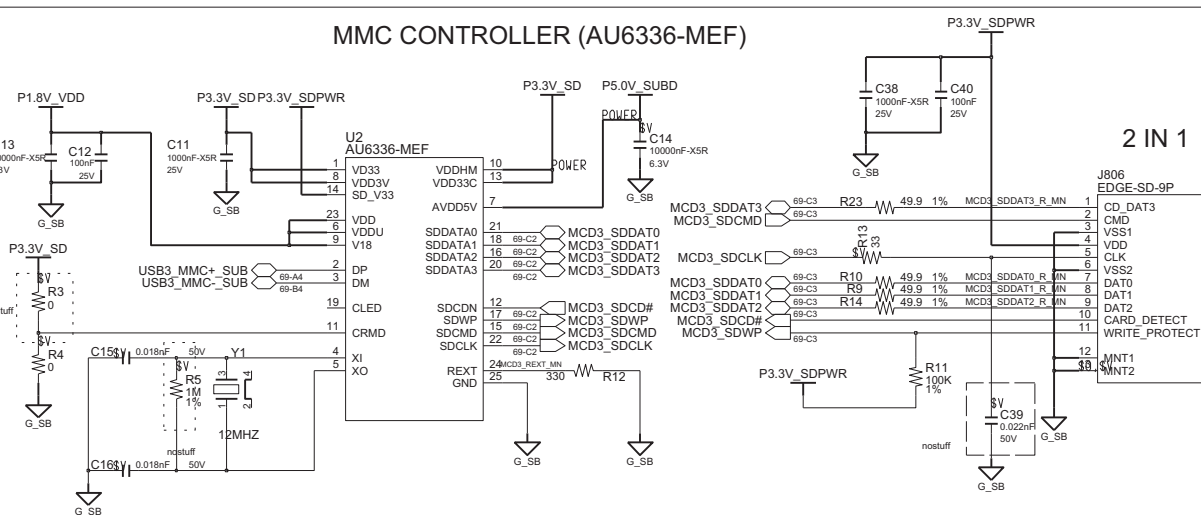
Audio Jack Sub Board



LID SWITCH



MMC CONTROLLER (AU6336-MEF)



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		CONFU		HANDBOOK TECH	
CHECK		DEV. STEP	MP						
APPROVAL		REV	1.0						
MODULE CODE		LAST EDIT		August, 16, 2009 3:24:04 PM		PAGE	38 OF 40		



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